## REMARKS

**Present Status of the Application**

The Office Action mailed January 14, 2004 rejected all presently pending claims 1-16 and 19-21. Specifically, claims 1-16 and 19-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Swonger (5,663,860) in view of Hwang et al. (5,273,915) and Yamaguchi et al. (6,118,154). Applicants have further amended claims 1, 8, 9, 14 and 21 to more clearly define the invention. Reconsideration of claims 1-16 and 19-21 is respectfully requested.

**Discussion of Rejections under 35 U.S.C. 103(a)**

One feature of this invention is that the single crystal silicon-side junction diode is electrically coupled between one terminal of a corresponding power supply and a node and dominates discharge of ESD current. The feature is recited in amended independent claims 1, 9, 14 and 21 as follows, marked by underlines.

1. An ESD protection structure ..... comprising:
an input resistor ..... ; and
at least a single crystal silicon-sided junction diode formed over the insulating material layer, wherein the single crystal silicon-sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node and dominates discharge of ESD current.

9. An ESD protection structure ..... comprising:
an input resistor ..... ; and
at least a single crystal sided junction diode formed over the insulating material layer, wherein the single crystal sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node and dominates discharge of ESD current.

14. A semiconductor structure of ESD protection, ..... comprising:
..... ;
an input resistor ..... ;
at least a single crystal Si-sided junction diode formed over the insulating layer, electrically coupled between one terminal of a corresponding power supply and the integrated circuit and dominating discharge of ESD current;

.....; and
a third conductive layer ..... .

21. An ESD protection structure ..... comprising:
an input resistor ..... ; and
a single crystal layer formed over the insulating material layer, wherein the single crystal layer comprises at least two doped regions with different dopant types to form a side junction diode, and the side junction diode is electrically coupled between one terminal of a corresponding power supply and a node and dominates discharge of ESD current.

Swonger fails to teach or suggest a single crystal silicon-side junction diode electrically coupled between one terminal of a corresponding power supply and a node and dominating discharge of ESD current. The Office Action indicated that Swonger teaches at least a single sided junction diode 26a formed over the insulating material layer 42 and electrically coupled between one terminal of a corresponding power supply 24 and a node 14. However, ***the terminal 24 is actually a ground voltage reference terminal*** (col. 4, line 23 and col. 7, line 8), but ***not a power supply as in this invention***.

In fact, Swonger teaches away from disposing a single crystal silicon-side junction diode between one terminal of a corresponding power supply and a node. As described in col. 4, lines 25-27, the voltage reference terminal 24 may more generally represent any voltage line ***through which discharging of high voltages appearing at pin 12 is desired***. Since it is impossible to discharge an ESD current through a power supply line, Swonger clearly precludes the possibility for the ground voltage reference terminal 24 to serve as a power supply.

Moreover, the diode 26a/b in Swonger is merely ***a bypass diode*** for bypassing and protecting the non-triggering SCR when the other SCR has been triggered, as described in col. 7, lines 24-43, which ***does not dominate discharge of the ESD current***. It is the ***SCR 28a/b*** that dominates discharge of the ESD current, while the SCR 28a/b is a combination of an NPN

transistor and a PNP transistor, as shown in FIG. 1B, but ***not a diode***.

The Office Action noticed that Swonger does not teach forming the device in a single crystal silicon, and cited Hwang et al. and Yamaguchi et al. to teach forming resistors in single crystal silicon and forming a single crystal silicon sided junction diode, respectively. However, neither Hwang et al. nor Yamaguchi et al. can cure the above discussed deficiencies of Swonger.

Therefore, combining Swonger with Yamaguchi et al. would merely replace the bypass diode 26a/b in Swonger with the sided junction diode of Yamaguchi et al., and ***the device dominating discharge of the ESD current in the resulting structure is still the SCR 28a/b, rather than a diode as in this invention***.

Therefore, even if Swonger, Yamaguchi et al. and Hwang et al. were combined as proposed, the combination would still fail to include all of the elements of the claimed invention.

For at least the reasons mentioned above, Applicants respectfully submit that amended independent claims 1, 9, 14 and 21 patently define over the prior art.

For at least the same reasons mentioned above, Applicants respectfully submit that claims 2-8 dependent from claim 1, claims 10-13 from claim 9, claims 15-16 and 19-20 from claim 14 also patently define over the prior art.

In addition, these dependent claims contain features that further distinguish over the cited references. For example, claim 8 recites a first diode and a second diode respectively connected to a first power supply and a second power supply. This feature is not taught or suggested by Swonger.

## CONCLUSION

For at least the forgoing reasons, it is believed that all pending claims 1-16 and 19-21 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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